REMARKS

Claims 1-40 are present in this application. Claims 1 and 14 are independent. Claims 35 to 40 have been added.

I. Allowable Subject Matter

Applicants wish to thank the Examiner for indicating that claims 33 and 34 are allowable.

II. Claim Rejection – 35 USC 102(b): Shyu

Claims 1, 3-6, 9-12, 14, 16-19, 22-25, and 27-32 are rejected under 35 U.S.C. 102(b) as being anticipated by WO 01/17030 (Shyu). Applicants traverse this rejection.

Embodiments pertaining to claim 1 are directed to a semiconductor memory comprising a p-type semiconductor film (e.g., silicon oxide film 14) provided on p-type semiconductor substrate (e.g., substrate 11), a p-type well region in a semiconductor substrate, or an insulator; a gate insulating film (e.g., insulating film 12) formed on the p-type semiconductor film; a single gate electrode (e.g., gate electrode 13) formed on the gate insulating film; two charge storage sections (e.g., charge storage sections 61, 62) formed on side walls of the gate electrode; a channel region (e.g., channel region 41, 42) provided below the gate electrode; a first n-type diffusion layer region and a second n-type diffusion layer region provided to sides of the channel region (diffusion layer regions 17, 18).

The Office Action alleges that control gate 114 teaches the claimed gate electrode, and that charge storage regions 116 and 126 teach the claimed two charge storage regions formed on side walls of the gate electrode.

Shyu discloses a "right charge storage region 116 on a right portion 118 of channel region 108 between center channel portion 112 and right diffusion region 104." Shyu discloses a "left charge storage region 126 on a left portion 128 of channel region 108 between center channel portion 112 and left

diffusion region 106" (see page 5, bottom two paragraphs). However, as can be seen in Figure 1 of Shyu, the right portion 118 and left portion 128 of the channel region 108, are located on either side of the sidewall areas of the dielectric composite layers. Thus, the right and left charge storage regions 116 and 126 are not formed on side walls of the gate electrode.

Furthermore, figure 1 of Shyu also shows a label 130, as apparently relating to a conductive layer over the structure shown in the figure. Shyu describes the lable 130 as pertaining to a polysilicon used as the word line (page 6, second paragraph). Shyu further describes the wordline 130 as being electrically connected to control gate 114 and is on top of the ONO dielectric composite layers. Figure 3H shows the final structure having the polysilicon layer 130. As can be seen in Figure 3H, the wordline 130 is in contact with the charge storage regions 116 and 126 of the ONO dielectric composite layers, as well as the control gate 114. In such case, it is apparent that the charge storage regions 116 and 126 together with the control gate 114 form an electrically integrated gate electrode.

For the above reasons, Applicants submit that Shyu fails to teach or suggest at least the claimed semiconductor memory including a single gate electrode, and two charge storage sections formed on side walls of the gate electrode, as required in the claims.

In addition, with respect to claims 27 to 32, Applicants submit that because Shyu fails to teach at least the claimed two charge storage section formed on side walls of the gate electrode, Shyu fails to teach the claimed "second part" of the charge storage film extending substantially parallel to a side face of the gate electrode. At least for this additional reason, Applicants submit that Shyu fails to teach each and every element of claims 27 to 32.

Accordingly, Applicants request that the rejection be reconsidered and withdrawn.

III. Claim Rejection – 35 USC 103(a): Shyu; Atsumi

Claims 2 and 15 have been rejected based on the combination of WO 01/17030 (Shyu) and again U.S. Patent 5,438,542 (Atsumi; previously applied). Applicants traverse this rejection.

Claim 2 is directed to the semiconductor memory of claim 1 as well as that the p-type semiconductor film is set to a voltage less than the reference voltage. The Office Action admits that Shyu fails to teach this claim limitation and instead relies on Atsumi for making up for this deficiency.

In particular, the Office Action states that Fig. 16 of Atsumi illustrates the claimed voltages. The Office Action states that it would have been obvious to one of ordinary skill in the art to utilize the collective data writing technique by means of substrate hot electrons of Atsumi in Shyu's semiconductor memory "in order to improve the efficiency of injecting electrons and allow simultaneous data writing for a plurality of memory cells to reduce the time required for a erasing/writing cycle test and for data writing before data erasure." Applicants disagree.

Atsumi and Shyu

Atsumi discloses a memory cell with a stacked gate structure and in particular, teaches a technique of hot electrons, while Shyu discloses a semiconductor memory having a two charge storage regions that correspond to a plurality of bits. In Shyu, programming is carried out by applying a high voltage to a diffusion region close to the charge storage region for storing the bit, while the region close to the other charge storage region has a low voltage applied. (see Shyu at paragraph bridging pages 6 and 7). In Atsumi, collective data writing by means of substrate hot electrons is carried out with both source and drain voltages set at ground potential. Writing using substrate hot electrons occurs when electrons accelerated by a depletion layer between the substrate and the channel are made to jump over the barrier of the gate oxide film and inject into the floating gate (col. 8, lines 21-24).

At least because the substrate hot electron technique of Atsumi requires voltages of both the source and drain to be at ground potential, Applicants submit that applying the technique of Atsumi to the semiconductor memory having two charge storage regions of Shyu would render Shyu unable to function to store the two bits. Accordingly, because of the substantial differences in structure and operation between teachings in Atsumi and Shyu, Applicants submit that one of ordinary skill would not have been

motivated to combine the teachings and the rejection thereby fails to establish *prima facie* obviousness. Applicants request that the rejection be reconsidered and withdrawn.

IV. Claim Rejection – 35 USC 103(a): Shyu, Yoshikawa

Claims 7, 8, 20, and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over WO 01/17030 (Shyu) in view of U.S. Patent 6,335,554 (Yoshikawa). Applicants traverse this rejection.

At least for the reasons above for claims 1 and 14, Applicants submit that the rejection fails to establish *prima facie* obviousness. Accordingly, Applicants request that the rejection be reconsidered and withdrawn.

V. Claim Rejection – 35 USC 103(a): Shyu; Eitan

Claims 13 and 26 have been rejected based on the combination of WO 01/17030 (Shyu) and again U.S. Patent 6,348,711 (Eitan). Applicants traverse this rejection.

At least for the reasons above for claims 1 and 14, Applicants submit that the rejection fails to establish *prima facie* obviousness. Accordingly, Applicants request that the rejection be reconsidered and withdrawn.

A. New Claims

Claims 35 to 40 have been added. The new claims cover further features of the disclosed invention and depend from claims 1 and 14.

At least for the reasons above for claims 1 and 14, Applicants submit that new claims 35 to 40 are patentable as well.

CONCLUSION

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination.

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but to merely show the state of the art, no comment need be made with respect thereto.

In view of the above amendments and remarks, reconsideration of the rejections and allowance of all of the claims are respectfully requested.

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (703) 205-8000 in the Washington, D.C. area.

A prompt and favorable consideration of this Amendment is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By _____
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